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Naphthalenetetracarboxylic Diimide Layer-Based Transistors with Nanometer Oxide and Side Chain Dielectrics Operating below One Volt

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ABSTRACT We designed a new naphthalenetetracarboxylic diimide (NTCDI) semiconductor molecule with long fluoroalkylbenzyl side chains. The side chains, 1.2 nm long, not only aid in self-assembly and kinetically stabilize injected electrons but also act as part of the gate dielectric in field-effect transistors. On Si substrates coated only with the 2 nm thick native oxide, NTCDI semiconductor films were deposited with thicknesses from 17 to 120 nm. Top contact Au electrodes were deposited as sources and drains. The devices showed good transistor characteristics in air with 0.1−1 μA of drain current at 0.5 V of V_G and V_{DS} and W/L of 10−20, even though channel width (250 μm) is over 1000 times the distance (20 nm) between gate and drain electrodes. The extracted capacitance-times-mobility product, an expression of the sheet transconductance, can exceed 100 nS V^{-1}, 2 orders of magnitude higher than typical organic transistors. The vertical low-frequency capacitance with gate voltage applied in the accumulation regime reached as high as 650 nF/cm^2, matching the harmonic sum of capacitances of the native oxide and one side chain and indicating that some gate-induced carriers in such devices are distributed among all of the NTCDI core layers, although the preponderance of the carriers are still near the gate electrode. Besides demonstrating and analyzing thickness-dependent NTCDI-based transistor behavior, we also showed <1 V detection of dinitrotoluene vapor by such transistors.

KEYWORDS: organic transistor · organic semiconductor · NTCDI · dielectric · sheet transconductance · capacitance · MIS · sensor

The field-effect transistor (FET) is the essential element in very large scale integrated (VLSI) microelectronics. Silicon FETs have evolved from the micro to the nano scale to accommodate requirements for faster computation and lower power consumption. The latest Intel microprocessor uses Si FETs with a 32 nm gate channel length.[1] While this shortened length enables higher area density of logic elements, the increased device density also depends on a scaled increase in gate capacitance by the combination of higher dielectric constant and lower gate thickness. In the 1990s and early 2000s, the electronics industry had reduced the thickness of SiO_2 used as the gate dielectric layer from 50 to 1.2 nm to reduce operating voltage and power consumption.[2−4] In 2006, Intel began selling the Pentium 4 core with 60 nm channel length and 1.2 nm of SiO_2 for the gate dielectric layer.

Similar considerations of power reduction, increased speed, and device density may apply to emerging organic electronics technologies. Organic semiconductors (OSCs) have contributed to new technologies such as organic light-emitting diodes (OLEDs), organic field effect transistor (OFET)-based circuits, and organic photovoltaics (OPV).[5,6] Among them, OLEDs are already commercialized for small displays such as in cellular telephones, and the others, including OFETs used in pixel switching, are in prototype stages or on the verge of market release.[7,8] OFETs are also under evaluation as environmental sensors and in identification tags, although multiple improvements are needed.[9−11] Low voltage and high response speed will be important for these as well.

Most early work on the electronic (as opposed to optoelectronic) properties of OSCs, for the development of OFETs,[12] was focused on bringing the field effect charge carrier mobility of OSCs to a value comparable to that of amorphous silicon, which has been the standard material for liquid crystal display (LCD) backplane circuitry. Thick SiO_2 (100−300 nm) has been widely used as a dielectric layer in OFETs to explore the performance parameters of OSCs such as mobility and on−off ratio because the oxide is easily obtainable and provides reproducible

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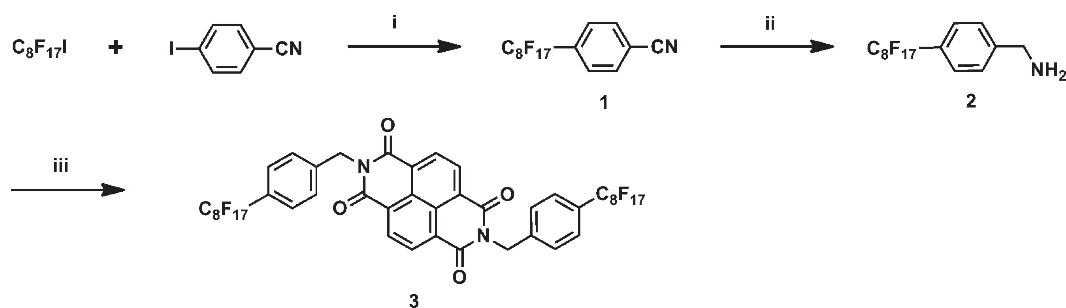

Scheme 1. Synthesis of new n-channel NTCDI. Conditions: (i) Cu, DMSO, 125 °C (ii) $BH_3 \cdot THF$, THF, reflux (iii) NTCDA, $Zn(OAc)_2$, quinoline, 190 °C.

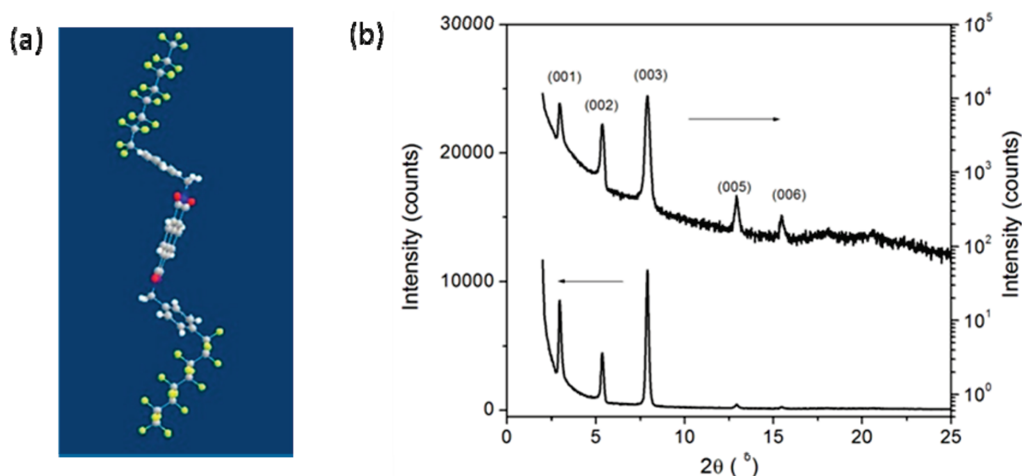

Figure 1. (a) Molecular simulation of 8-0-Bn-NTCDI. (b) XRD patterns for the 8-0-Bn-NTCDI film deposited at 130 °C on native oxide/n^{++} Si substrate: linear (left) and log (right) scales.

conditions to many OFET researchers.[12] More recently, attention has also been paid to OFET dielectric layers in order to increase reliability and decrease operating voltage of OFETs.[13] Thus in the last 10 years, many groups have studied high capacitance dielectric layers in order to scale down dimensions of organic devices compared to those using Si−SiO_2 technology.[13] They have used very thin amorphous polymers,[14] SAM-treated[15−17] or polymer-treated inorganic dielectrics,[18] polymer electrolyte dielectrics,[19] and high k inorganic dielectrics.[20] Finally some groups have achieved 1 V operating OFETs.[18,20]

OSCs contain conjugated rings as a ubiquitous structural element. OSCs of OFETs also frequently comprise insulating side chains in order to increase crystallite sizes, control crystal orientations and morphologies in thin films, alter solubilities of solid film materials, and/or stabilize OSCs to the environment.[21−23] Charge carriers can tunnel through or past the side chains before being transported within layers of conjugated cores in OSCs. Interactions of side chains with environmental chemicals also influence sensing activity of OFETs.[24,25]

In this article, we explore the dielectric activity of a particular type of side chain attached to a naphthalenetetracarboxylic diimide (NTCDI) conjugated core. While attempts have been made to produce OFETs from single layers of molecules that included both a dielectric side chain and a conjugated subunit,[26,27] this is the first study to determine contributions of side chains to gate capacitance depending on the numbers and possibly positions of side chains in multilayer stacks. Such devices reveal new insights about the relative contributions of charge carrier mobility and gate capacitance as a function of the number of layers. Except for a 2 nm native oxide on a heavily doped silicon substrate gate, no other dielectric is deposited. This lowers operating voltages significantly because of the much higher capacitance between the channel and the gate. A separate dielectric deposition step is avoided, and a highly homogeneous, and possibly intramolecular, dielectric−OSC interface is achieved because layers of the same molecular structures deposited in a single vapor deposition step serve as both the dielectric and OSC. The choice of NTCDI for the core adds additional advantages of electron transport capability and transparency, as has already been well recognized.[28]

RESULTS AND DISCUSSION

Design and Synthesis of NTCDI. Scheme 1 represents the synthesis of the *bi*functional NTCDI OSC, which we designate as 8-0-Bn-NTCDI. The starting material for attaching the desired side chain, perfluorooctylbenzylamine,

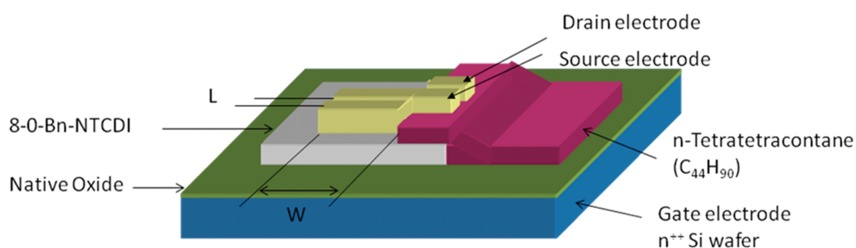

Figure 2. Device configuration of low-voltage OFET on the native oxide.

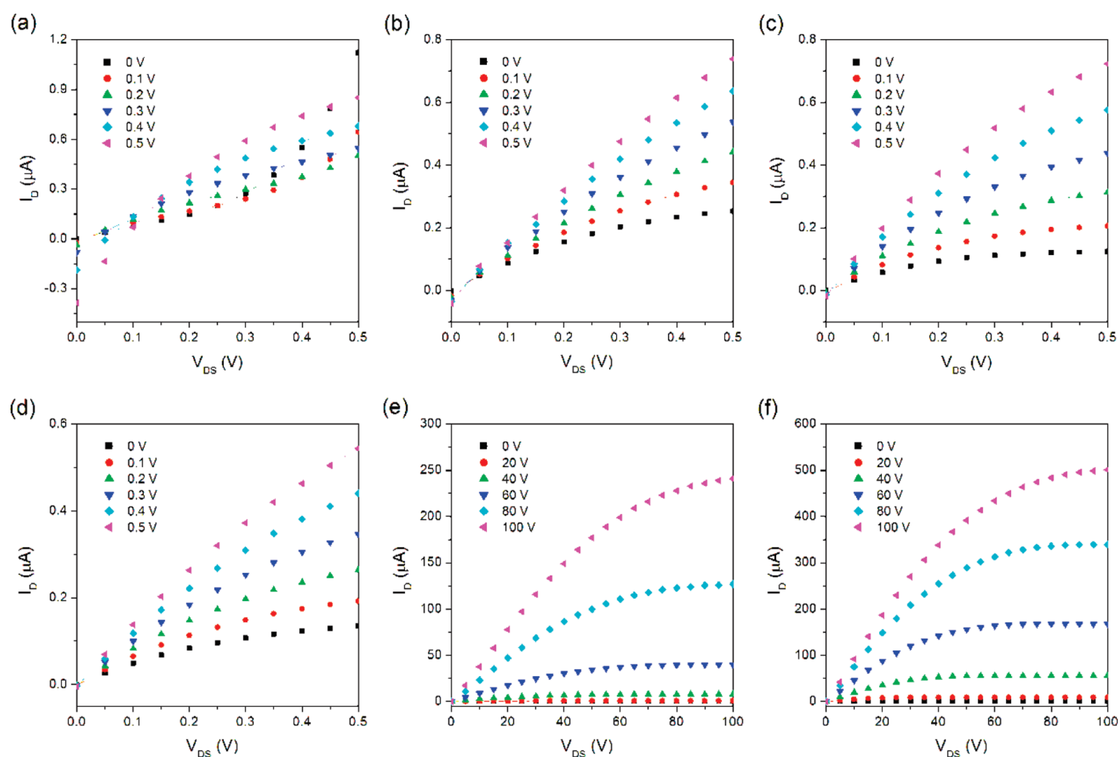

Figure 3. Typical output characteristic curves (I_D *vs* V_{DS}) with various V_G in ambient conditions: (a) 13 nm (4 MLs), (b) 17 nm (5 MLs), (c) 20 nm (6 MLs), and (d) 30 nm (9 MLs) of NTCDI device on the native oxide, (e) 13 nm (4 MLs) and (f) 17 nm (5 MLs) of NTCDI device on the 300 nm oxide. OFETs of (a)−(d) have a channel width (*W*) of 2000 μm and a channel length (*L*) of 150 μm, and OFETs of (e) and (f) have 8000 and 150 μm for *W* and *L*, respectively.

is not commercially available but can be synthesized in just two steps. First, the reaction of perfluorooctyl iodide, 4-iodobenzonitrile, and copper in DMSO provides a reasonable yield of perfluorooctylbenzonitrile.[29,30] This is converted to the desired amine by refluxing with $BH_3 \cdot THF$ complex in THF.[31] The side perfluorooctylbenzyl group is isolated electrically from the conjugated core because the phenyl ring and the core are connected *via* a methylene linker. The molecular length of the new NTCDI was calculated to be 3.31 nm through MOPAC simulation, as shown in Figure 1a. The *d*-spacing determined by X-ray diffraction (XRD) from the NTCDI thin film is 3.36 nm, identical within the limits of experimental uncertainty. The missing fourth-order peak, which occurs in films of multiple thicknesses, is likely an indication of structure factor cancellations. Therefore, it is likely that the NTCDI molecules stand up from the substrate as illustrated in Figure 1a. A terraced morphology was observed analogously to other common OSC films, and the height of one layer was between 3 and 4 nm (Figure S1). This is further evidence that the 3.36 nm layer thickness from the XRD result is the thickness of one monolayer of 8-0-Bn-NTCDI.

Device Fabrication. We fabricated low-voltage transistors from 8-0-Bn-NTCDI on doped Si, topped with its native oxide, following the precedent of Halik *et al.*[15] We opted not to append the special self-assembled monolayer (SAM) to the native oxide because we expected that the side chain of the NTCDI would act as an additional dielectric layer, as though it were a SAM, shielding the NTCDI core layers from leakage paths to the gate. After piranha solution cleaning, a 2 nm thickness of the native oxide was measured by ellipsometry, a value similar to other reported thicknesses.[32] The thickness of deposited NTCDI layers ranged from 13 nm, roughly 4 MLs, to 120 nm. To prevent the direct contact of probes with the source and drain

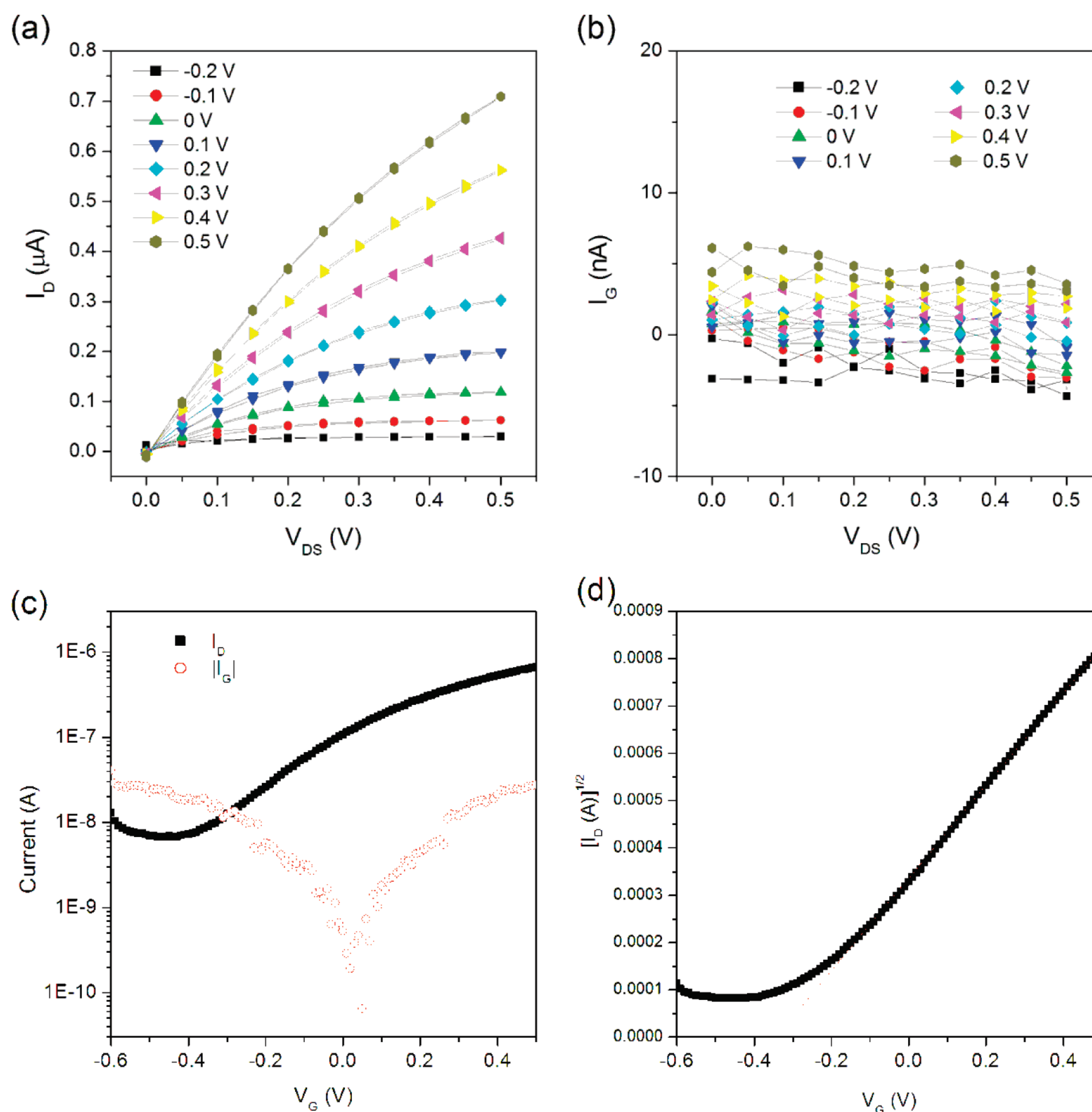

Figure 4. (a) Hysteresis curves for output characteristics (I_D *vs* V_{DS}) with various V_G in ambient conditions of 20 nm (6 MLs) of NTCDI device on the native oxide with *W/L* of 2000 μm/150 μm. (b) Corresponding gate leakage. (c) Transfer characteristics (I_D *vs* V_G) at VDS of 0.5 V. (d) $I_D^{1/2}$ *vs* V_G curve.

through to the native oxide because of puncturing, we deposited at least 40 nm of an insulating material, tetratetracontane ($C_{44}H_{90}$),[33] on one side of the NTCDI multilayer using a metal shadow mask and then deposited 60 nm of Au as the source and drain electrodes extending from the tetratetracontane covering layer out toward the NTCDI (Figure 2). Some devices made from thick NTCDI on the native oxide without the insulating layer under the Au electrode pads did show FET behavior because it was possible to make delicate contact between the probe and Au electrodes. The total thickness including the Au and NTCDI layer, often less than 100 nm, was so thin that the sharp manually controlled probes easily penetrated them. When the probe contacted the native oxide, the device was short-circuited at the start of a measurement due to the high gate leakage current, even when only 0.1 V was applied. With the insertion of the tetratetracontane layer, we increased the probability of a successful measurement from 20% to 70%. Wire bonding remains as a possible alternative to the tetratetracontane layer.

Besides the ultrathin device architecture, we made OFETs on octadecyltrimethoxysilane (OTS)-treated 300 nm thick SiO_2 on Si as a comparison for mobility and capacitance−voltage measurements. We also used 8-3-NTCDI[34] with a linear semifluorinated chain ($-C_3H_6C_8F_{17}$) and 8-2-Bn-NTCDI, analogous to compound **3** but with a side chain longer by two methylene carbons between the perfluoroalkyl and phenyl groups, for comparison devices.

Device Performance. Figure 3 shows the typical output characteristic curves of two kinds of devices, differing by the thickness of the NTCDI. The transistors with >16 nm of NTCDI (5 MLs) on the native oxide operate well at

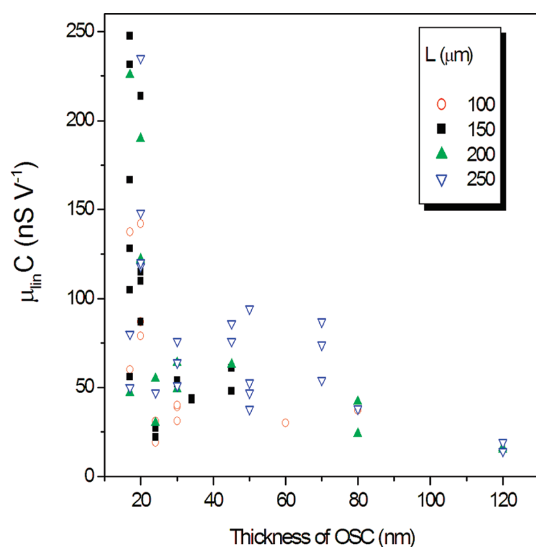

Figure 5. OFET sheet transconductances as a function of the thickness of the OSC (8-0-Bn-NTCDI). All devices were in the configuration shown in Figure 2, with different spacings between the source and drain electrodes. Widths were 2−3 mm.

voltages < 0.5 V, compared those on 300 nm of SiO_2, which need several tens of volts for operation. Devices with only 13 nm (4 MLs) of NTCDI on the native oxide showed some FET currents modulated by V_G beyond 0.3 V. However, high leakage currents, probably through pinholes under the electrodes, overwhelmed drain-source current (I_{DS}) at gate voltages (V_G) < 0.2 V. At $V_G = 0$, the sweep of V_D from 0 to 0.5 V means increasing V_{DG} from 0 to 0.5 V. Therefore, the diode-like behavior at 0 V of V_G defines the leakage current of a metal−insulator−semiconductor (MIS) structure. The current−V_D curve at 0.5 V of V_G showed field-effect enhancement, but the current at 0 V of V_D was not the desired 0 μA, but −0.4 μA, representing the leakage current from −0.5 V of V_{DG}. The 13 nm (4 MLs) device on thick (300 nm) SiO_2 showed the field-effect behavior without any leakage current behavior at V_D = 0 V or V_G = 100 V, in contrast to the 13 nm device on native oxide. After depositing 17 nm (5 MLs) or more of NTCDI on the native oxide, we achieved FET characteristics with lower gate leakage currents. The currents at 0.5 V of V_G and V_D were still not zero. *However, in the case of thicker NTCDI, these were now field-effect currents arising from a negative threshold voltage, perhaps arising because of an interface dipole, rather than gate leakage.*

The 20 nm (6 MLs) devices showed clearly saturating FET currents increasing with increasing V_D and off states at −0.2 V of V_G as in Figure 4. This device on the native oxide exhibited negligible hysteresis, even though the device was measured in the ambient environment. This behavior is another example of the fluorooctylbenzyl side chain in the OSC molecules increasing air stability like other reported n-channel NTCDIs.[22,34] When 8-3-NTCDI[34] with a linear semifluorinated chain ($-C_3H_6C_8F_{17}$) was deposited on the native oxide, the device was leaky. The difference in molecular structures between 8-0-Bn-NTCDI and 8-3-NTCDI is the spacers, which are the benzyl ($-CH_2C_6H_4-$) and propyl ($-C_3H_6-$) groups, respectively. The successful blocking of the leakage current of 8-0-Bn-NTCDI is attributable to the aromatic ring, perhaps related to the effect of the special SAM with a phenoxy group described by Halik *et al.*, which they found to be very helpful for fabrication of a low-voltage OFET.[15] A significant achievement of our device is that the simultaneously recorded I_G was <10 nA, much less than I_D, without any SAM treatment on the native oxide, as shown in Figure 4b. Therefore, I_D *ca.* 100 times higher than I_G was obtained for the 0.5 V of V_G and V_D through the field effect, even though the lateral electric field of 3.3 × 10^{-5} MV/cm (= 0.5 V/150 μm) is much smaller than the vertical electric field of 0.22 MV/cm (= 0.5 V/22 nm). Thus, our device is among those with the least possible gate dielectric among reported OFETs.

The negative threshold voltages were obtained from the typical I_G−V_G transfer curve, holding V_D at 0.5 V, using one of following two principal FET equations:[13]

$$I_{DS} = \frac{W}{L} C_i \mu_{lin} \left[(V_G - V_T)V_D - \frac{V_D{}^2}{2} \right] \quad \text{Linear region} \tag{1}$$

$$I_{DS} = \frac{W}{2L} C_i \mu_{sat} (V_G - V_T)^2 \quad \text{Saturation region} \tag{2}$$

where *W* is the channel width and *L* the channel length, μ the field effect carrier (in this case electron) mobility of the semiconductor, C_i the capacitance per unit area of the gate insulator, V_G the gate voltage, V_T the threshold voltage, and V_D the drain voltage. It is difficult to achieve at least μA of drain current from OFETs operating at 1 V or lower with conventional thick SiO_2 (100−300 nm). Because a C_i of 100 nm of SiO_2 is only 35 nF cm^{-2}, if 1 V of V_G were applied to OFETs with 0 V of V_T and *W*/*L* of 20, saturated drain current would be limited to <35 nA for the OSC with 0.1 cm^2 V^{-1} s^{-1} of mobility on over 100 nm of SiO_2 dielectric layer. However, our devices using bifunctional semiconducting molecules attain nearly microampere currents at voltages below 0.5 V.

In the low-voltage OFETs with dielectric layers other than thick SiO_2, performance comparison is somewhat difficult because of the difficulty in isolating mobility and capacitance effects. Therefore, some investigators suggest the capacitance times mobility (C_i × μ) product as a preferable parameter.[18] This product can be called "sheet transconductance", and its unit is nS V^{-1} from nF cm^{-2} × cm^2 V^{-1} s^{-1}. For example, we obtained 144 nS V^{-1} of sheet transconductance for the 20 nm (6 MLs) device in Figure 4. This value is much

TABLE 1. Summary of the Capacitance and OFET Characteristics for Low-Voltage n-Channel OFETs

measurement condition	dielectric layer	OSC	C_i (nF cm^{-2})	μ (cm^2 V^{-1} s^{-1})	sheet transconductance (nS V^{-1})	V_T (V)	on/off ratio	ref
air	Al_2O_3 + SAM	$F_{16}CuPc$	700	0.02	14	−0.2[a]	10^5	16
	SAND	DFHCO-4TCO	300	0.02	6	−0.6	10^3	35
	polymer + cross-linker	$F_{16}CuPc$	165	0.045	7.4	0.38	10^3	36
	native oxide + one side chain of OSC	8-0-Bn-NTCDI	650	0.22	144	−0.34	10^2	this work
inert gas or vacuum	HfO_2 + SAM	C_{60}	580	0.28	162	0.35	10^5	37
	Al_2O_3 + polymer	C_{60}	50	2.5	125	0.2	10^6	38
	ionic liquid	C_{60}	~5000	~0.06[b]	~ 340[c]	0.4	10^4	39

[a] Assumed value from the data. [b] This mobility is the linear region mobility. [c] This value is different from the calculated value from the tabulated $C_i \times \mu$. Authors of ref 37 used rounded numbers for each value.

higher than 3 or 4 nS V^{-1} from the devices on 300 nm SiO_2 with 0.3−0.4 cm^2 V^{-1} s^{-1} of mobility. We plot this value for a large number of devices in Figure 5. The very highest values of sheet transconductance, on the order of 200 ns V^{-1}, are reproducible, as shown in Supporting Information, Figure S2.

There are some previously reported low-voltage pentacene p-channel OFETs with several hundred nS V^{-1} of sheet transconductance using SAM on the native oxide and high *k* dielectric layer,[15−17] self-assembled molecular thickness/nanoscale gate dielectrics (SANDs),[35] or thin polymer dielectrics.[36] These devices have required at least −1 V of V_G to operate due to high V_T. Using those methods, the researchers fabricated n-channel OFETs and achieved 14 or 7.4 nS V^{-1} for $F_{16}CuPc$[16,34] and 6 nS V^{-1} for DFHCO-4TCO[33] under ambient conditions because of relatively low mobility compared to that of pentacene. Some groups reported over 100 nS V^{-1} from C_{60} n-channel OFETs under vacuum or inert atmosphere.[37−39] Our device exhibits comparable n-channel sheet transconductance to C_{60} OFETs, even though it was measured in air. Eventually, this type of device could also be used a gas sensor with low operating voltage, and the demonstration will be discussed below. The performance of various low voltage n-channel OFETs is summarized in Table 1.

Insights from Capacitance Measurements and Carrier Concentration Calculations. We have explored sheet transconductance of the devices on the native oxide as a function of the thickness of NTCDI in the linear region because some devices did not show clear saturation within 0.5 V of V_G and V_D due to the large negative V_T. Sheet transconductances decrease with the increased thickness, as is apparent from Figure 5. Some researchers have reported the performance as a function of the thickness of OSC layers in the conventional SiO_2 dielectric OFETs.[40−44] The mobilities were generally saturated after several MLs or a thickness of less than 20 nm. This phenomenon was first explained using the solution to Poisson's equation under the assumption that the gate-induced carriers are mostly located at the interface between OSC layers and the dielectric.[45,46] This solution is a function of the Debye length, and for most OSCs, the Debye length is <1 nm depending on the dielectric constant of the OSC and total induced charges.[47]

If the capacitance of the dielectric in our device were constant like those of conventional OFETs (35−10 nF cm^{-2}), our results would represent the variation of mobility with the thickness. Therefore, to determine the origin of the trend of sheet transconductance in our devices, we measured the capacitance dependence on bias voltage for an MIS structure (n^{+2}-Si/native oxide/8-0-Bn-NTCDI/Au) and a capacitor comprising just the native oxide (Figure 6). The native oxide exhibited leakage current with applied voltage beyond ±0.1 V, so that the values beyond this range are invalid for judging the true capacitance. The measured capacitance (1000 nF cm^{-2}) for the native oxide at 0 V is lower than the calculated capacitance (1730 nF cm^{-2}) for 2 nm of SiO_2 (dielectric constant, k = 3.9) from the standard eq 3, but this is commonly observed in ultrathin SiO_2 structures.[48]

$$C_i = \varepsilon_0 \frac{k}{d} \quad (3)$$

In the above, ε_0 is the vacuum permittivity, k is the dielectric constant, and d is the thickness. The capacitance−voltage curve for an MIS structure with 20 nm NTCDI (6 MLs) shows the typical MIS capacitor characteristics with the depletion and accumulation region. The capacitance in the accumulation region reaches 650 nF cm^{-2}, somewhat less than that of the native oxide. This capacitance is consistent with an additional dielectric layer lying on the native oxide. The calculated length of one fluorooctylbenzyl side chain is 1.2 nm. Assuming the dielectric constant of the side chain is the same as that of Cytop, a well-known fluorinated dielectric polymer,[49] the value of the calculated capacitance of one side chain is 1550 nF cm^{-2} according to eq 3. The total series capacitance for the native oxide and one side chain is calculated to be 610 nF cm^{-2} from eq 4 (Figure 6c).

$$\frac{1}{C_{tot}} = \frac{1}{C_1} + \frac{1}{C_2} \quad (4)$$

This value is close to the measured capacitance in the accumulation region in the C−V curve, allowing for

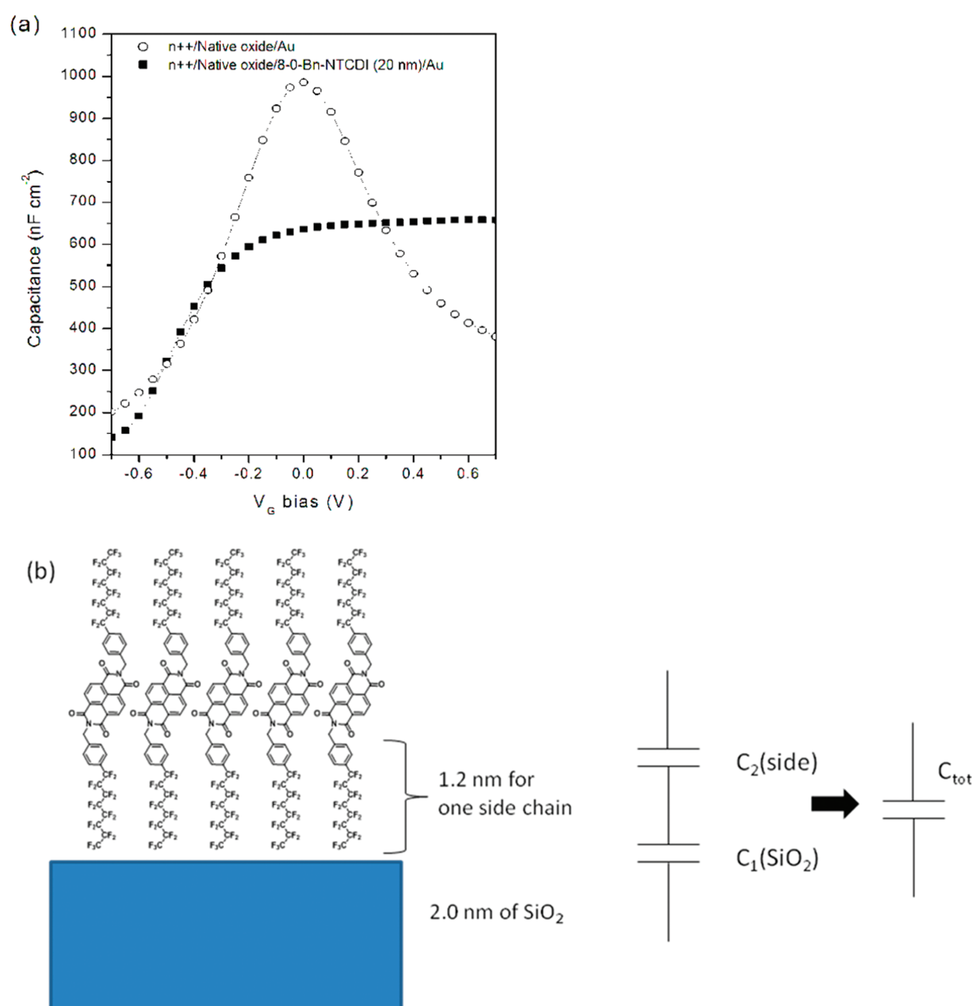

Figure 6. Capacitance *vs* bias voltage (a) at 20 Hz (the lowest available frequency) for n^{++}-Si/native oxide/8-0-Bn-NTCDI (20 nm)/Au. (b) Schematic structure for our device and equivalent circuit.

uncertainty in the estimation of the side chain dielectric constant. This correlation supports our hypothesis that the side chain functions as part of the dielectric. Furthermore, it suggests that at least some of the charges induced by gate voltage are distributed to all the NTCDI layers (6 MLs) or that all the layers have at least some modest conductivity under the top electrode. Otherwise, a capacitance as high as 650 nF cm^{-2} could not be achieved because of additional series capacitance from the insulating NTCDI layers. The additional capacitance of even one NTCDI layer (3.36 nm) is less than 790 nF cm^{-2} when the dielectric constant is assumed to be below 3, so the resulting series capacitance of this layer and the native oxide would be 450 nF cm^{-2} or less. Therefore, we conclude that the conducting part of our thin devices includes all the NTCDI layers except the bottommost side chain.

The observation by other groups of "saturation" of the "mobility" with the thickness does not necessarily mean that the charges are in the first two layers, just that adding more layers does not provide more efficient current paths.[43,44,50] Horowitz[47] proposed that carriers would be distributed according to the thermodynamic equilibrium governed by the limits of how many charge carriers can reside on individual molecules and how many can be confined in individual layers, in the case of layered OSC OFETs. This proposal is somewhat different from the model for amorphous OFETs[45] in which carriers would be locally distributed according to Poisson's equation without as severe a geometric restriction. However, direct experimental evidence for these conjectures has not yet been reported. Our results, particularly the high capacitance we observe, along with our application of the Horowitz theoretical model to our own system (see Supporting Information), provide new evidence that significant carrier concentrations may indeed be found in layers above that second one, *although it must be emphasized that this "upper layer" carrier density is still only a small fraction of the total charge.* The calculated charge density of the sixth layer as a function of V_G showed a functional form similar to the corresponding experimentally obtained $C-V$ curve (Figures S3c and 6). Perhaps the charge density calculated for this layer in the "on" state, between 10^{10} and

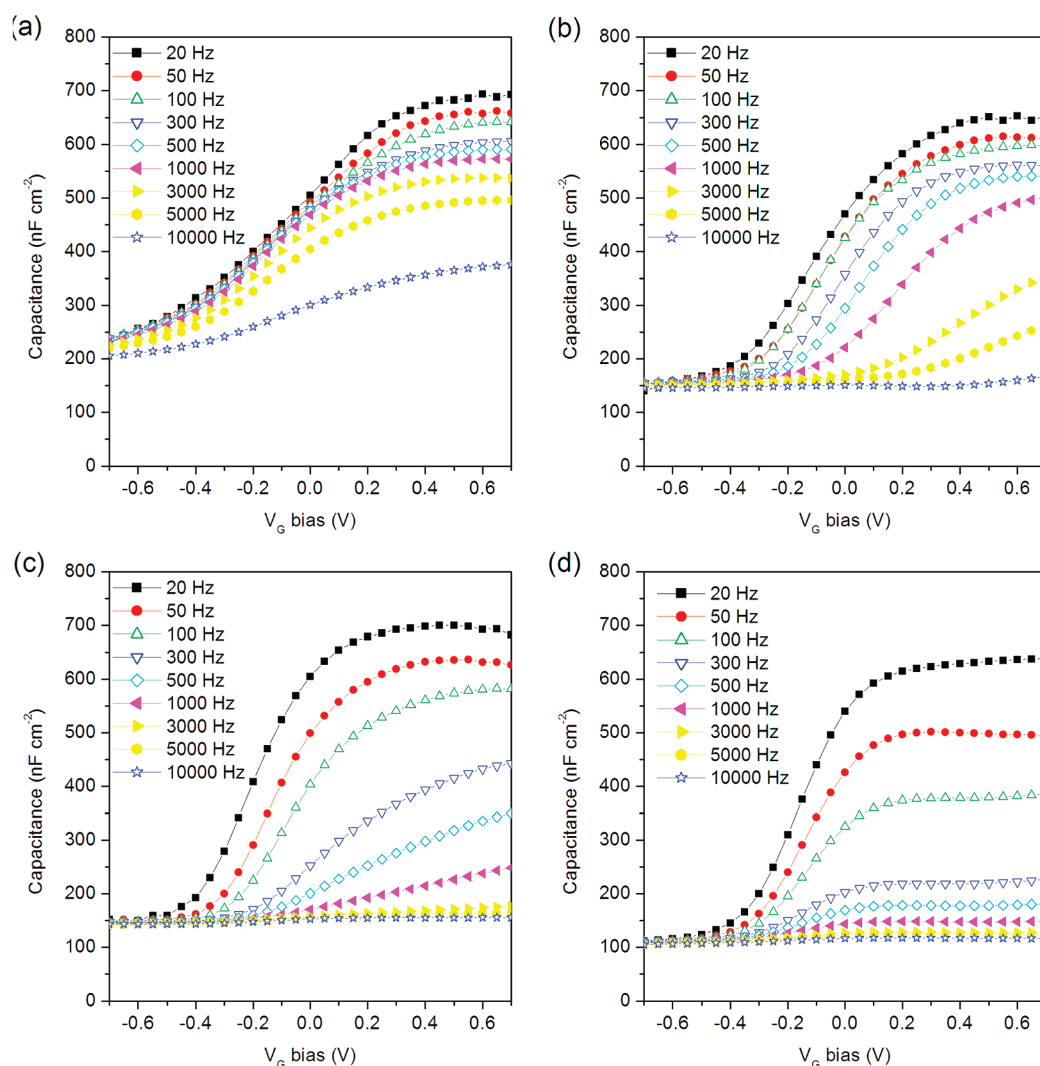

Figure 7. Frequencies-dependent capacitance−voltage curves of MIS diodes with (a) 17 nm (5 MLs), (b) 20 nm (6 MLs), (c) 24 nm (7 MLs), and (d) 34 nm (10 MLs).

10^{11}/cm^2, corresponds to a minimum charge density for full conduction in each layer, leading to the maximum capacitance of the multilayer stack.

Figure 7 shows the frequency-dependent $C-V$ characteristics as a function of the thickness of the OSC. A plot of frequency dependence of capacitance at constant accumulation-regime voltage for each thickness is displayed in Figure S4. At 20 Hz, the lowest tested frequency, the capacitances in the accumulation region were ca. 650 nF cm^{-2} for MIS devices with 17 to 34 nm of NTCDI. The devices exhibited decreasing capacitance with increasing frequency in the accumulation regime. This was also observed for other OSCs[51,52] and explained by the slow redistribution of charges at higher frequencies. The thicker devices showed rapidly deceasing capacitance with frequency. Our low-voltage transistors were tested using 1 ms pulsed gate voltage to reduce the gate bias effect during measurements. Decreased sheet transconductance after 24 nm (6 MLs) of NTCDI is related to this rapid decreasing capacitance at high frequency. When 0.1 s pulsed gate voltage was used instead, I_{DS} increased, because the capacitance at that longer time scale was increased. We conclude that the sheet transconductance dependence on the OSC thickness in our devices was affected by the frequency-dependent capacitance. The capacitive and resistive components that determine the relaxation frequency f_R are indicated *via* equations in the Supporting Information.[51,53] For frequencies below f_R, the measured capacitance is the insulator capacitance, and for frequencies above f_R, it drops to the series sum of the insulator capacitance and OSC capacitance, as in the depletion regime. From the frequency-dependent $C-V$ curves, we can extract the dopant density using Mott−Schotty analysis of the variation of capacitance in the depletion regime (Figures S5 and S6).[52,54] However, this would be related to the subthreshold slope rather than the sheet transconductance of the transistor.

We showed that a related but slightly longer semifluorinated alkylbenzyl NTCDI,[55] (8-2-Bn-NTCDI,

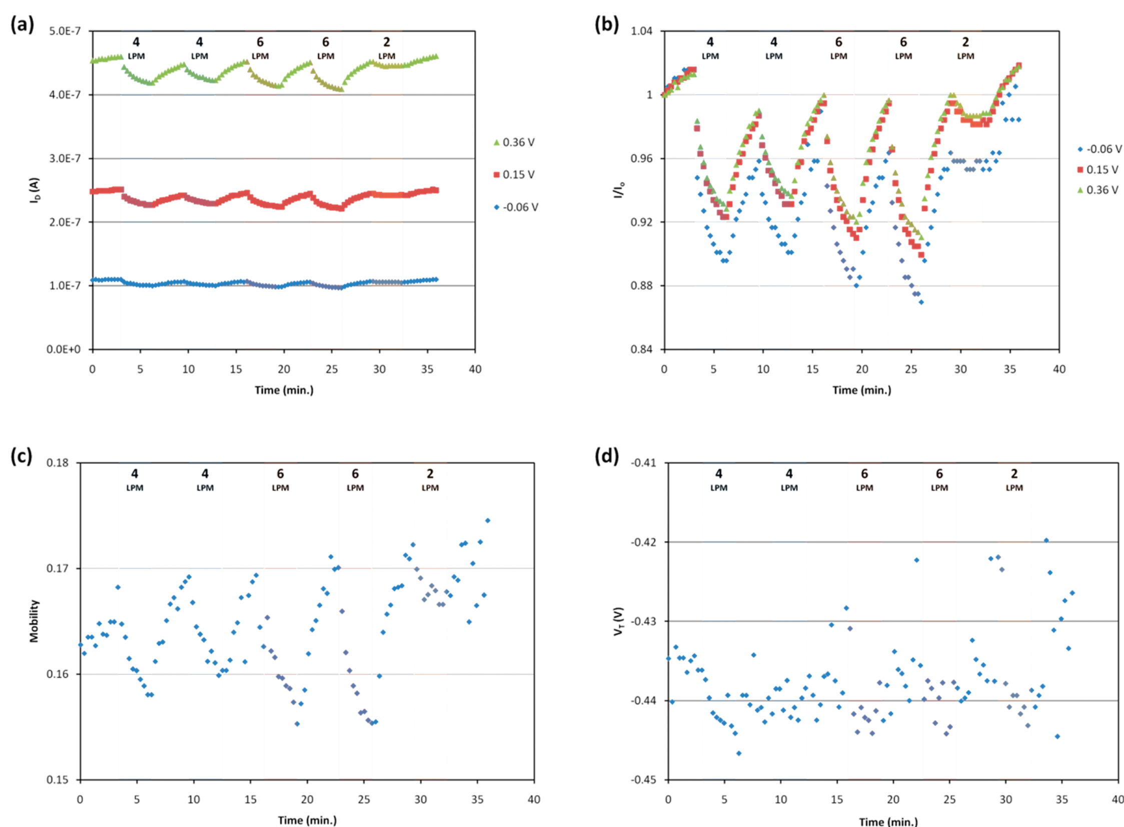

Figure 8. OFET response with 20 nm 8-0-Bn NTCDI on the native oxide upon exposure to DNT vapors at various concentrations. LPM refers to the flow rate of dry air over the DNT solid; 0.5 V of V_D was applied for operation in the saturation region. (a) Response of drain currents at different V_G. (b) Normalized response of drain currents referenced to initial currents. (c) Response of mobility. (d) Response of threshold voltage.

standing for octylethylbenzyl-NTCDI) also performed well on the native oxide (see Supporting Information, Figure S7). The performance of the device was not explored in the same depth as for 8-0-Bn-NTCDI devices, but shows that the observations in this study are not a special effect of a single compound. The relative length of the 8-2-Bn side chain versus the 8-0-Bn side chain is 1.25 not counting the benzyl group, or 1.17 counting the benzyl group, and the two dielectric constants are very similar. Rounding to 1.2 relative dielectric thickness, the side chain capacitance of the longer side chain is lower by 20% compared to that for the shorter side chain. The total series capacitance of one 8-2-Bn side chain plus the oxide is 550 nF cm^{-2}, 85% of the capacitance of the 8-0-Bn side chain plus the oxide. This is within the scatter of Figure 5 and in good agreement with the low-voltage capacitance value from Figure S7c.

The decrease in both capacitance and capacitance-mobility product for thicker films suggests that at kHz frequencies and above many of the thick-film layers are insulating. For example, in a 34 nm (10 MLs) MIS structure, we obtained a much lower capacitance, <150 nF cm^{-2} in the accumulation region (Figure 7d). If this value reflects true dielectric capacitance, it would explain the decreasing sheet transconductance with film thickness. We calculate mobilities by assuming that all but two NTCDI layers are in fact part of the dielectric, in addition to the native oxide. We are not certain of why there seems to be a "critical" change at this 7 ML thickness, but perhaps that is the thickness at which the layers below become essentially defect-free, meaning no leakage paths and also no penetration by the top source/drain contacts. We also cannot be certain whether the uppermost or the bottommost layers are dielectric-like and which of the layers behave like semiconductors, but our experiments and the Horowitz model are both consistent with the channel forming in upper regions of the films, while lower layers are insulating. The mobility that we calculate with this assumption, on the order of 1 cm^2 V^{-1} s^{-1}, is appropriate for the NTCDI used, with well-formed grains and a clean interface that would be expected from the channel being formed on a "dielectric" of identical molecules at an identical purity. This compares to the mobility of about 0.2 cm^2 V^{-1} s^{-1} we obtained for the devices on 300 nm of oxide (Figure 3e and f). However, our experiments cannot rule out an equilibrated state with some OSC layer capacitance between the top electrode and the channel, and an additional capacitance under the accumulation layer leading to the gate electrode.

The critical thickness of OSC above which sheet transconductance decreases toward values for more

"conventional" OFETs can depend on the oxide quality. When the native oxide after piranha solution cleaning was left in air for over 3 weeks, a 34 nm (10 MLs) device exhibits over 100 nS V^{-1}, similar to 20 nm (6 MLs) devices (Figure S8). However, a 34 nm (10 MLs) device from the fresh native oxide showed 44 nS V^{-1}, as did other thick NTCDI layer devices.

Application to Sensor Technology. We tested our 20 nm NTCDI device on the native oxide as a sensing element for nitroaromatic explosive-derived vapor. As shown in Figure 8, the devices at only 0.5 V of V_{DS} successfully exhibited a response upon exposure to dinitrotoluene (DNT) vapors. The delivery system described in a previous report[56] was used to deliver DNT vapor at various concentrations. I_D was recorded as the output signal as a function of time. Field-effect mobility and threshold voltage were extracted and also plotted *vs* time. The shadowed areas indicate the DNT vapor exposure periods. The current response exhibited gate voltage dependence when it was normalized with the initial current. An additional plot showing this, in the form of transfer curves, is in Figure S9. At lower gate voltage, the relative current changed more upon exposure to DNT. This may be related to the carrier distribution among the layers, dependent on the gate voltage, as discussed in above. The carriers at the low gate voltage are more widely distributed away from the gate than those at high V_G. The relative carrier concentration close to the top surface at low V_G is higher than at the high V_G. There should be a higher response of the relative current at low V_G than high V_G due to the greater interactions of carriers in upper layers with DNT vapors.

SUMMARY AND CONCLUSION

We investigated films of a novel core-unsubstituted NTCDI OSC ranging from 13 nm, corresponding to that of 4 MLs, to 120 nm in thickness. Electronic characterization was performed on OFETs and capacitors using silicon with its native oxide as the substrates, with no other dielectrics. Mobilities of 0.1−1 $cm^2 V^{-1} s^{-1}$ were obtained in air from OFETs operating below 1 V, and a response to dinitrotoluene vapor was obtained. Evidence for side chain monolayers in thin devices, and NTCDI multilayers in thick devices, contributing to the gate dielectric was obtained. Charge distributions were calculated consistent with both experimental data from this study and the theoretical model for multilayer OSCs proposed by Horowitz. Better definition of the carrier distribution, including some frequency-dependent data, contributes greatly to understanding performance mechanisms and limitations, especially for multifunctional devices such as sensors. The films represent a model system from which other bifunctional (dielectric plus semiconductor) molecular assemblies for low-voltage, transparent electronic devices may be derived.

METHODS

Materials. 4-Perfluorooctylbenzonitrile (**1**) was synthesized according to the previous report.[30] 4-Perflourooctylbenzylamine (**2**) and *N,N'*-bis(4-perflourooctylbenzylamine)-1,4,5,8-naphthalenetetracarboxylic diimide (**3**) (and the perfluorooctylethyl analogue) were synthesized using modified or similar procedures.[31,57]

4-Perflourooctylbenzylamine (2). To 4-perfluorooctylbenzonitrile (2.66 g, 5.10 mmol) in 60 mL of anhydrous THF was added 25.5 mL of 1 M $BH_3 \cdot THF$ dropwise at room temperature. The mixture was heated to reflux for 1 day and cooled to room temperature. Then 100 mL of 2.6 M HCl was carefully added and refluxed for 30 min. After cooling, the white salt was filtered. The white solid was basified with NaOH(aq), and the amine was extracted with ethyl acetate. This extract was washed with brine, dried over $MgSO_4$, and concentrated as a viscous, yellow oil (1.71 g, 64%). ^{1}H NMR ($CDCl_3$, 400 MHz): δ 7.56 (d, 2H, J = 8.4 Hz), 7.47 (d, 2H, J = 8.4 Hz), 3.96 (s, 2H).

N,N'-Bis(4-perflourooctylbenzylamine)-1,4,5,8-naphthalenetetracarboxylic Diimide (3, 8-0-Bn-NTCDI). 4-Perflourooctylbenzylamine (1.27 g, 2.42 mmol), naphthalenetetracarboxylic dianhydride (NTCDA, 0.216 g, 0.81 mmol), and zinc acetate (0.111 g, 0.605 mmol) were mixed in 8 mL of quinoline. The mixture was heated at 190 °C overnight under N_2. Excess methanol was added and stirred at room temperature. The solid was filtered and washed with acetone. The crude solid was stirred in hot Na_2CO_3(aq) for 4 h and filtered. After washing with methanol and acetone, the product was purified twice by vacuum sublimation as a white solid (0.72 g, 70%). Elemental analysis conducted by Atlantic Microlab (Norcross, GA): Calcd for $C_{44}H_{16}F_{34}N_2O_4$: C, 41.20; H, 1.26; N, 2.18. Found: C, 41.12; H, 1.21; N, 2.29.

Device Fabrication. The highly n-type doped silicon wafers (As-doped Si wafer, ⟨100⟩, 0.001−0.007 ohm-cm) were cut into 1 in. × 0.5 in. substrates. The substrates were placed into piranha solution (sulfuric acid and 30% of hydrogen peroxide 3:1 mixture (*Danger! Highly corrosive and oxidizing*)) for 30 min. The wafers were cleaned by ultrasonication in deionized water, acetone, and 2-propanol followed by N_2 blowing and 10 min of 100 °C baking. After the substrates were moved to the vacuum evaporator, 8-0-Bn-NTCDI was deposited at a substrate temperature of 130 °C under 10^{-5} mbar at 0.02−0.1 nm s^{-1} until the desired thickness (13−120 nm) was reached. A tetratetracontane layer (40 nm) was deposited on one region of the NTCDI layer, and Au electrodes with channel widths of 3 or 2 mm and lengths ranging from 100 to 250 μm were deposited, crossing both the tetratetracontane and NTCDI layer surfaces. For MIS structures, Au top electrodes of 6.5 mm^2 were deposited. OFETs on OTS-treated SiO_2 were fabricated similarly to the previous report.[34]

Electrical Measurements. OFETs were evaluated using an Agilent 4155C semiconductor analyzer in air. The capacitance of the MIS devices was measured using an Agilent 4284A LCR meter using a test signal of 20 mV. For the DNT vapor sensing test, dry air was used as a carrier. X-ray diffraction scans were acquired in Bragg−Brentano (theta−2theta) geometry using a Phillips X-pert Pro X-ray diffraction system.

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Supporting Information Available: AFM image of the 8-0-Bn-NTCDI film, considerations of charge density in each layer, and estimation of mobilities from the measured sheet transconductance; transfer curves for DNT vapor sensing. These materials are available free of charge *via* the Internet at http://pubs.acs.org.

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